WHAT IS CLAIMED IS:

1. An execution control apparatus of a data driven information processor, wherein a handled instruction includes N + 2 (N is an arbitrary integer of at least 1) inputs at most, and one of the inputs is a constant when an instruction has N + 2 inputs, said execution control apparatus comprising:

an instruction decoder that decodes an instruction in an input packet and outputs the number of inputs required for said instruction;

a waiting storage region including

a waiting data storage region that can store N waiting data in one address, and

a data valid flag storage region that stores a data valid flag for each address, said data valid flag indicating whether the N waiting data stored in said address are respectively valid or invalid;

a constant storage device including

a region that stores a constant, and

a constant valid flag storage region that stores a constant valid flag representing whether a constant stored in each address is valid or invalid;

a constant readout unit that accesses said constant storage region according to address information included in an input packet to read out a constant and a constant valid flag from the relevant address in said constant storage region;

a waiting operation determination unit that determines an address by hash calculation from contents of the input packet, selects one of a plurality of predetermined ways of processes for waiting data, outputs a select signal depending upon a combination of a data valid flag for said determined address, a constant valid flag read out by said constant readout unit, and the number of instruction inputs output from said instruction decoder for said waiting storage region, and updates the data valid flag for said address based on the selected result; and

a waiting region access unit being responsive to said select signal to

implement a waiting process corresponding to said select signal.

2. The apparatus according to claim 1, wherein said constant storage region includes a first constant storage region that stores constant data of a first type, and a second constant storage region that stores constant data of a second type,

wherein said constant readout unit identifies whether the readout constant is of said first type or said second type according to the address.

3. The apparatus according to claim 2, wherein
said constant data of the first type is a scalar constant, and
said constant data of the second type is a vector constant.

4. The apparatus according to claim 3, wherein
each packet can store plurality of data, and
said waiting operation determination unit can store a plurality of data for each packet.

5. The apparatus according to claim 2, wherein
said constant data of the first type is a scalar constant of a first length, and
said constant data of the second type is a scalar constant of a second length different from said first length.

6. The apparatus according to claim 1, wherein N of said data valid flags are prepared for one address.

7. The apparatus according to claim 6, wherein each data valid flag is prepared of one bit for one waiting data of one address, and
said data valid flag storage region includes N flip-flop circuits for each address, each flip-flop circuit storing a data valid flag of one bit.

8. The apparatus according to claim 1, wherein said data valid flag

storage region includes an erasable storage circuit that clears the region in response to a reset signal.

9. The apparatus according to claim 8, wherein each of data valid flag is prepared of one bit for one waiting data of one address, and

said erasable storage circuit includes a D flip-flop circuit for each address, each D flip-flop circuit storing a data valid flag of one bit.

10. The apparatus according to claim 1, further comprising an input number detection unit that, when the number of inputs is N+2, updates the constant valid flag to a value representing "invalid", updates the number of inputs to N + 1, and outputs the updated constant valid flag and the updated number of inputs to the waiting processing unit.

11. The apparatus according to claim 1, wherein N = 2.

12. The apparatus according to claim 1, wherein N = 1.

13. An execution control method of a data driven information processor, wherein a handled instruction includes N + 2 (N is an arbitrary integer of at least 1) inputs at most, and one of the inputs is a constant when an instruction has N + 2 inputs, said data driven information processor comprising:

an instruction decoder that decodes an instruction in an input packet to output the number of inputs required for said instruction;

a waiting storage region including

a waiting data storage region that can store N waiting data in one address, and

a data valid flag storage region that stores a data valid flag for each address, said data valid flag indicating whether the N waiting data stored in said address are respectively valid or invalid;

a constant storage device including

a region that stores a constant, and

a constant valid flag storage region that stores a constant valid flag representing whether a constant stored in each address is valid or invalid;

a constant readout unit accessing said constant storage region with a node number of an input packet as an address to read out a constant and a constant valid flag from the relevant address in said constant storage region;

a waiting operation determination unit that determines an address by hash calculation from contents of a packet, selects one of a plurality of predetermined ways of processes for waiting data, outputs a select signal corresponding to a combination of a data valid flag for said determined address, a constant valid flag read out by said constant readout unit, and the number of instruction inputs output from said instruction decoder for said waiting storage region, and updating the data valid flag for said address based on the selected result; and

a waiting region access unit being responsive to said select signal to implement a waiting process corresponding to said select signal,

said method comprising the steps of:

decoding an instruction, wherein an instruction in an input packet is decoded by said instruction decoder, and the number of inputs required by the instruction is output;

reading out a constant, wherein said constant storage region is accessed based on address information included in the input packet, and a constant and a constant valid flag are read out from a relevant address in said constant storage region;

determining a waiting process, wherein an address is determined by hash calculation from contents in the packet, one of a plurality of predetermined ways of processes for waiting is selected, a select signal is output corresponding to a combination of a data valid flag for said address, a constant valid flag read out from said constant readout unit, and the number of instructions output from said instruction decoder for said waiting storage region, and the data valid flag is updated corresponding to said address based on the selected result; and

executing the waiting process, wherein, in response to said select

signal, a waiting process corresponding to said select process is performed.

14. The method according to claim 13, wherein said constant storage region includes a first constant storage region that stores constant data of a first type, and a second constant storage region that stores constant data of a second type,

wherein said step of reading out a constant includes the steps of:

determining as to whether the constant is of said first type or said second type based on the address, and

reading out the constant.

15. The method according to claim 14, wherein

said constant data of the first type is a scalar constant, and

said constant data of the second type is a vector constant.

16. The method according to claim 14, wherein

said constant data of the first type is a scalar constant of a first length, and

said constant data of the second type is a scalar constant of a second length differing from said first length

17. The method according to claim 13, said data valid flag storage region including an erasable storage circuit clearing the region in response to a reset signal,

said method further comprising the step of applying a reset signal to said storage circuit, thereby clearing said data valid flag storage region.

18. The method according to claim 13, further comprising the step of updating said constant valid flag to a value representing "invalid" and said number of inputs to N + 1 and applying said updated values to said waiting processing unit when said number of inputs is N + 2, after said step of reading out a constant and before said step of determining a waiting process.

19. The method according to claim 13, wherein N = 2.

20. The method according to claim 13, wherein N = 1.